

FIG.1(a) prior art

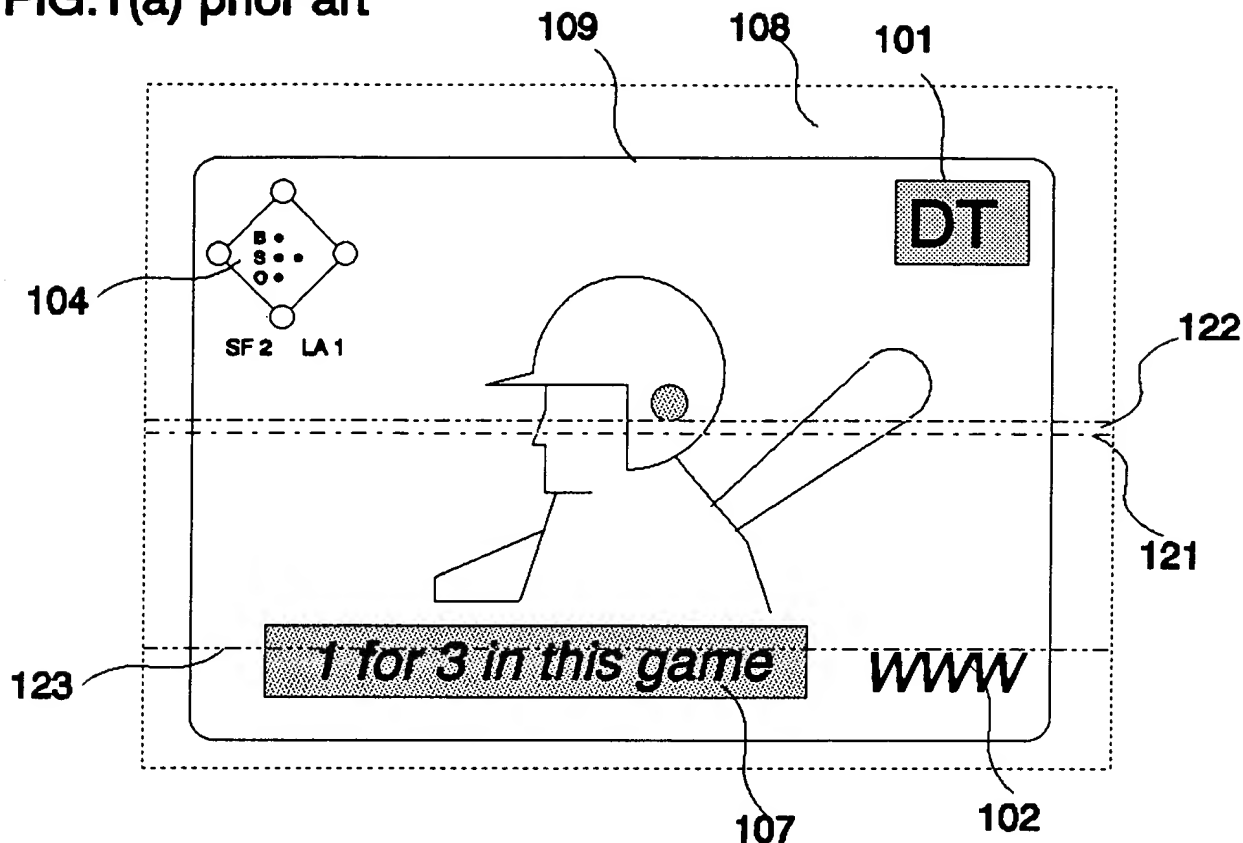


FIG.1(b) prior art

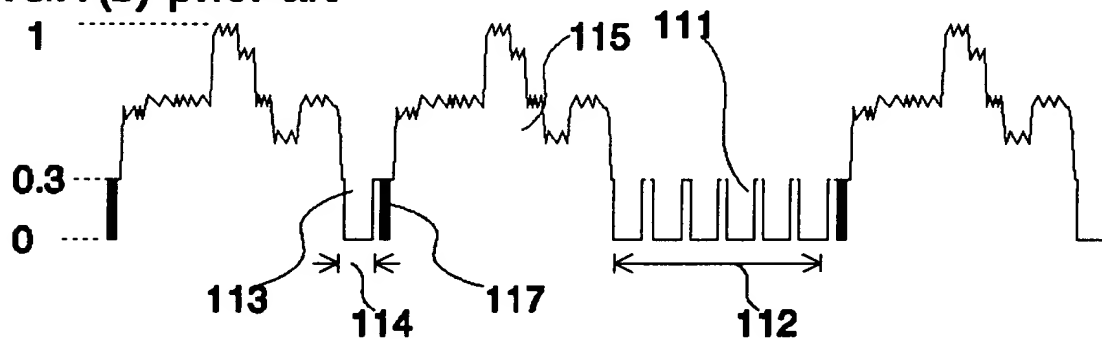


FIG.1(c) prior art

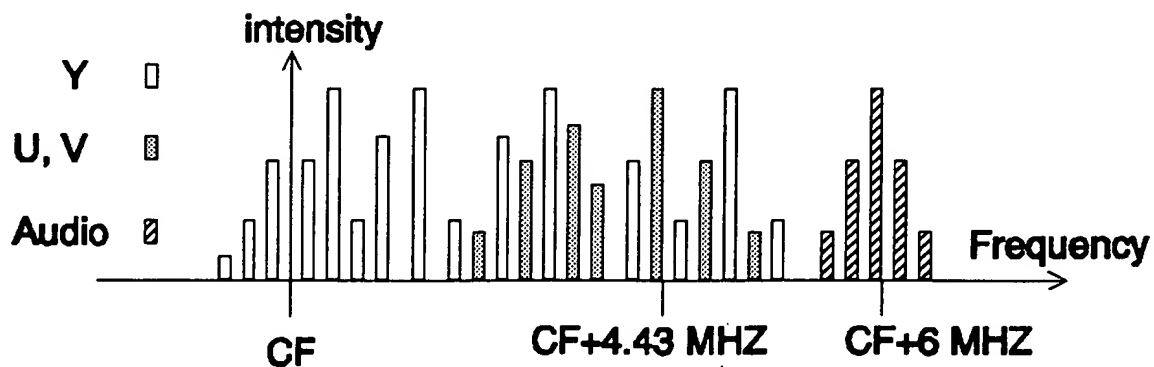


FIG.1(d) prior art

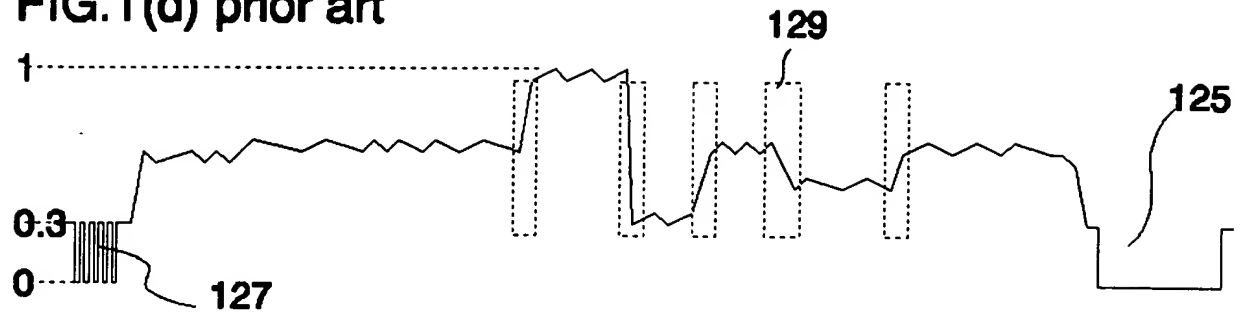


FIG.1(e) prior art

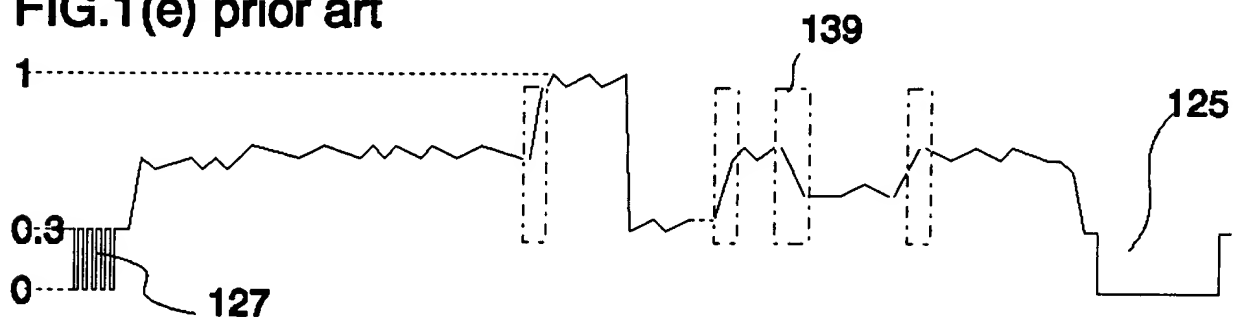


FIG.1(f) prior art

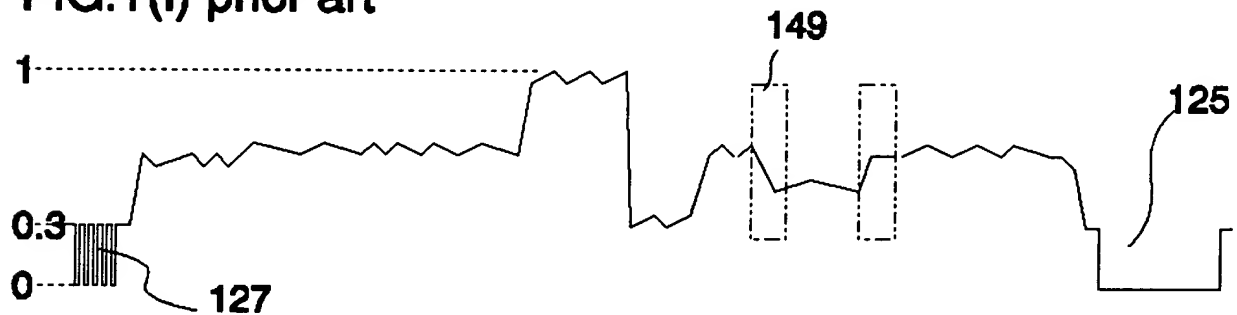
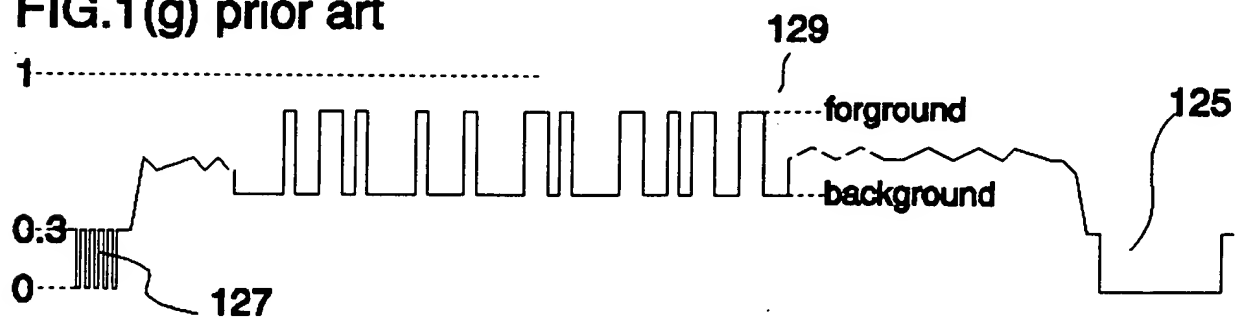


FIG.1(g) prior art



**FIG.2(a)**

A cross-sectional view of a semiconductor device structure. The structure consists of a substrate 125 with a series of vertical lines on its left side. A layer 0.3 is deposited on top of the substrate. A layer 201 is formed on top of layer 0.3, with a dashed line indicating its boundary. A layer 1 is formed on top of layer 201, with a dashed line indicating its boundary. A layer 201 is formed on top of layer 1, with a dashed line indicating its boundary. A layer 125 is formed on top of layer 201, with a dashed line indicating its boundary.

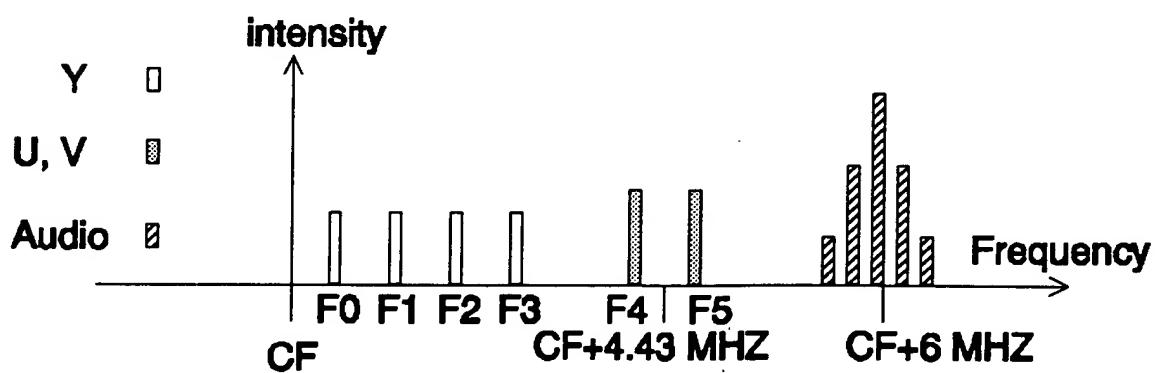
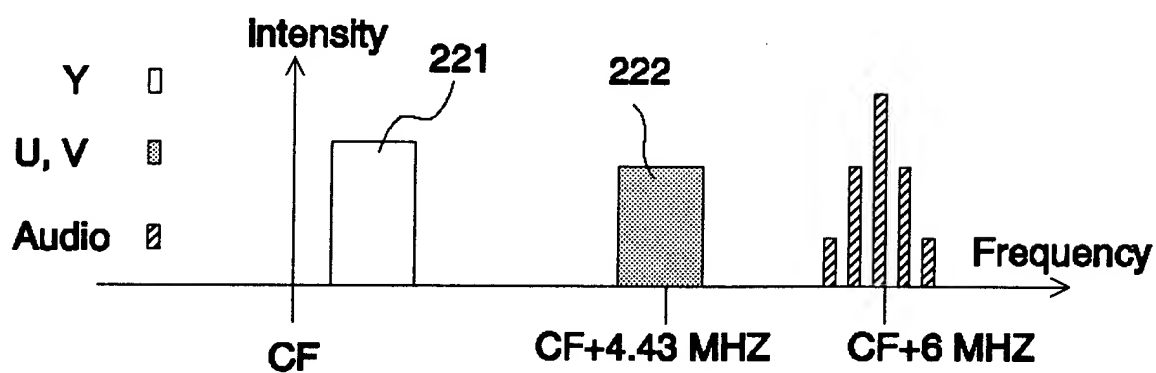
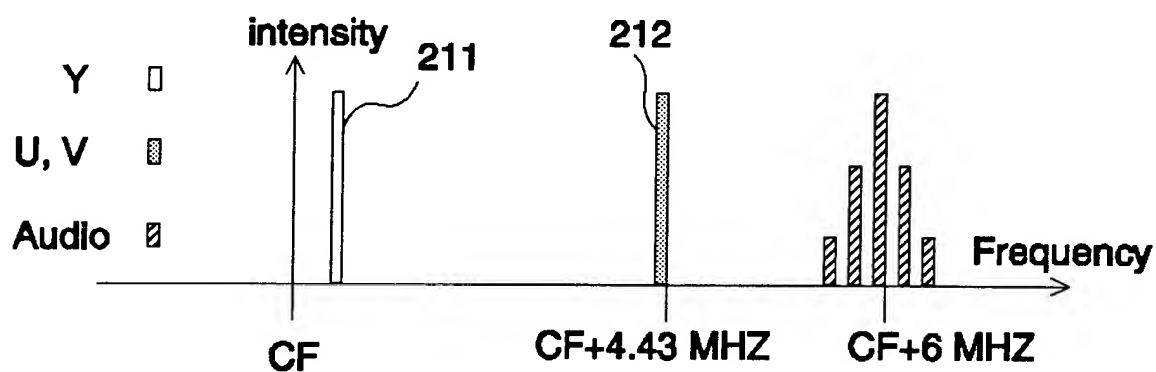


FIG.2(e)

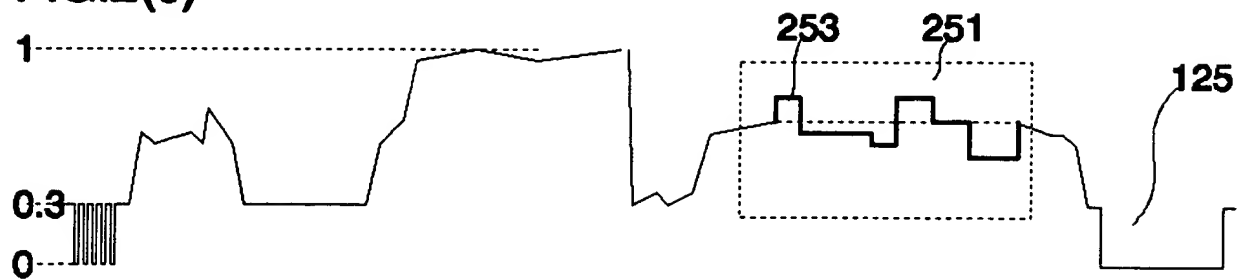


FIG.2(f)

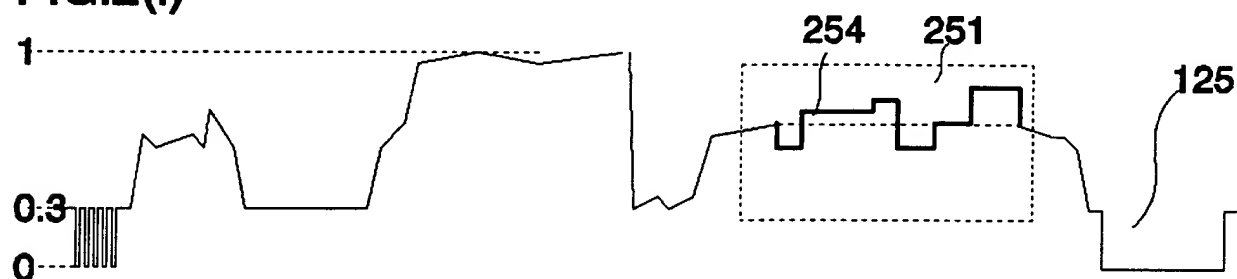


FIG.2(g)

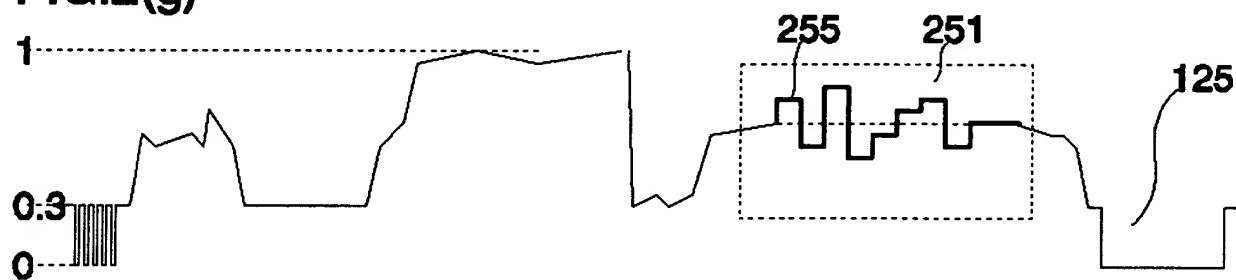


FIG.2(h)

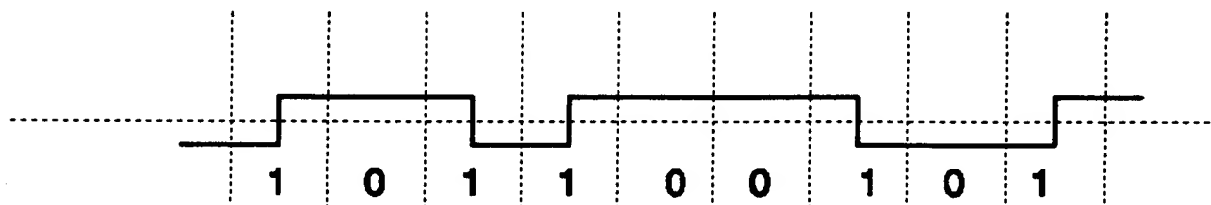




FIG.4(a)



FIG.4(b)



FIG.4(c)

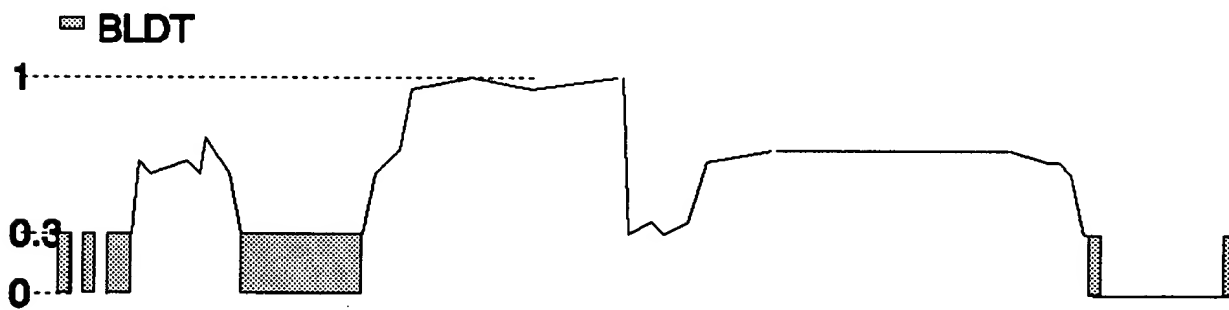


FIG.5(a)

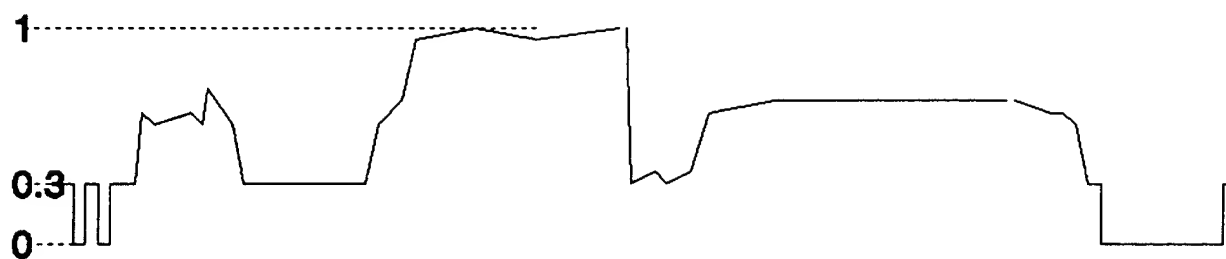


FIG.5(b)



FIG.5(c)

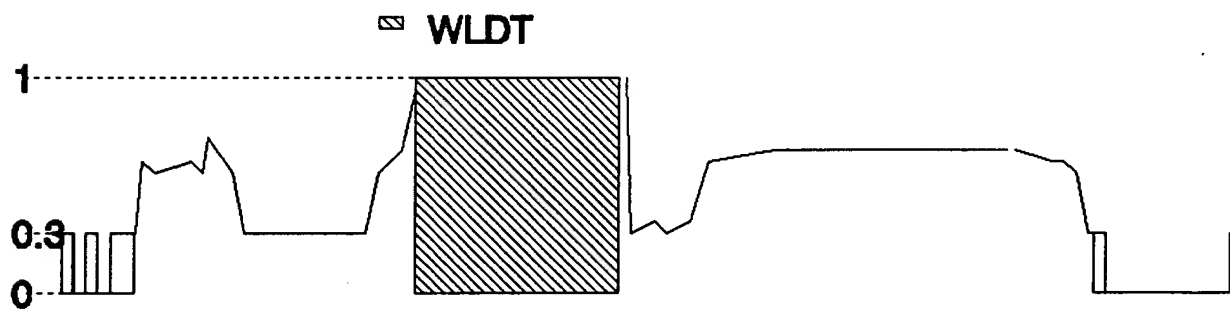


FIG.6(a)

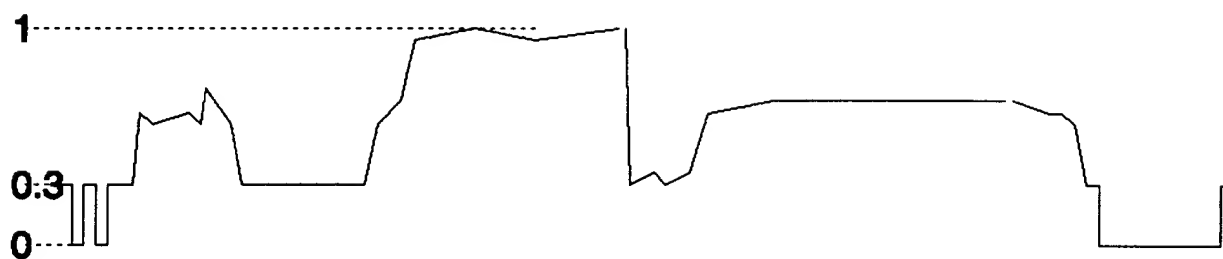


FIG.6(b)

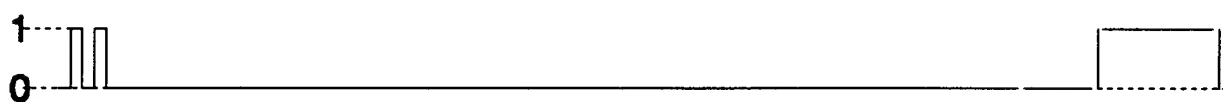


FIG.6(c)

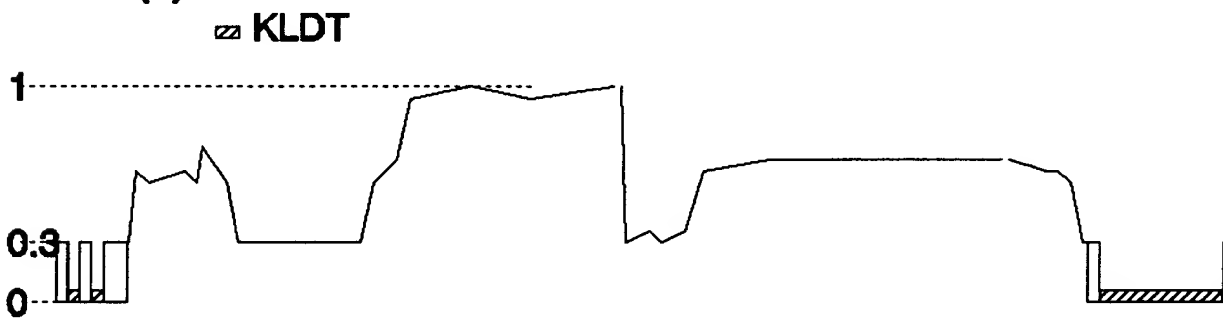




FIG. 7(a)

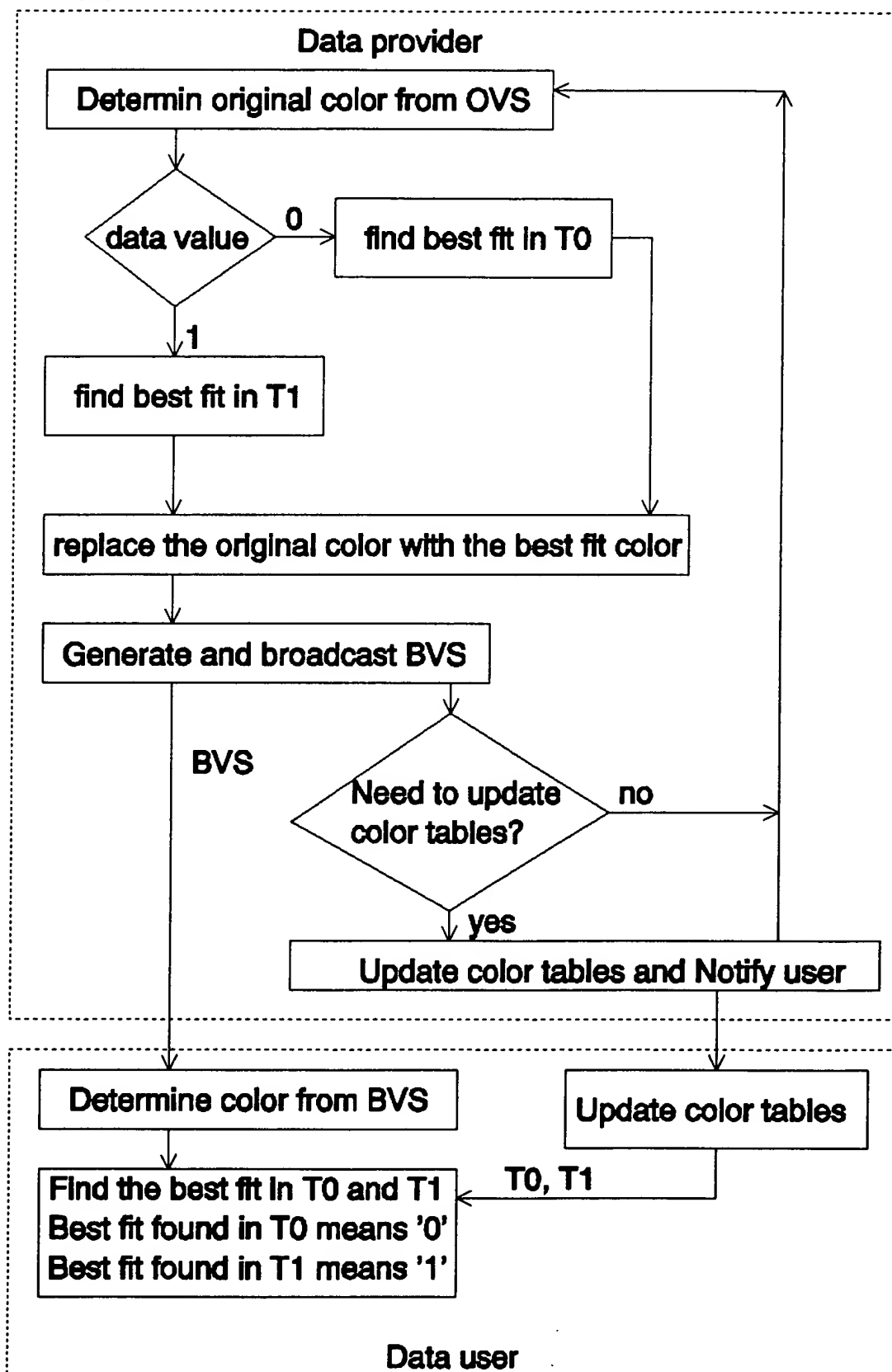


FIG. 7(b)

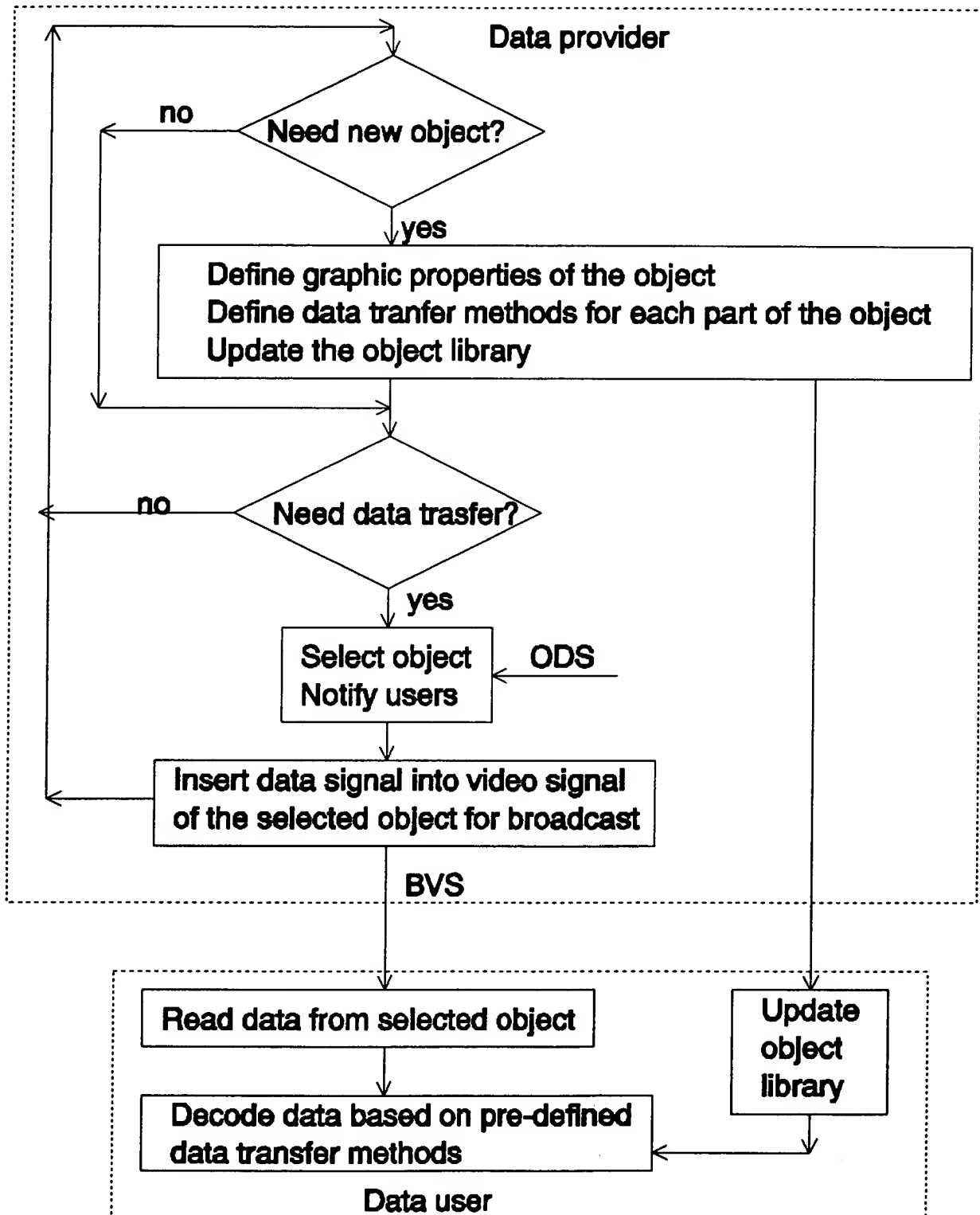
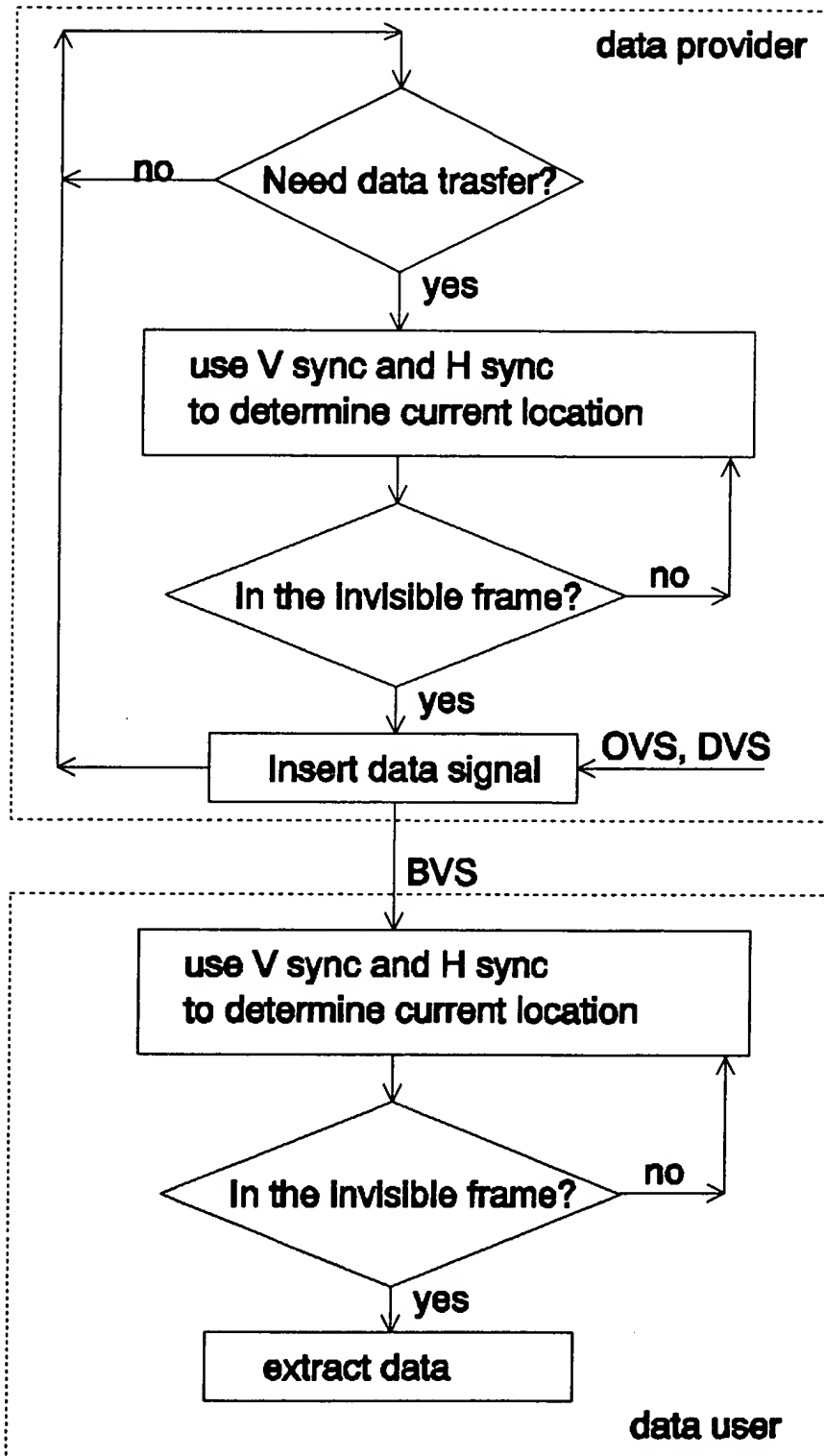


FIG. 7(c)



**FIG. 8(a)**

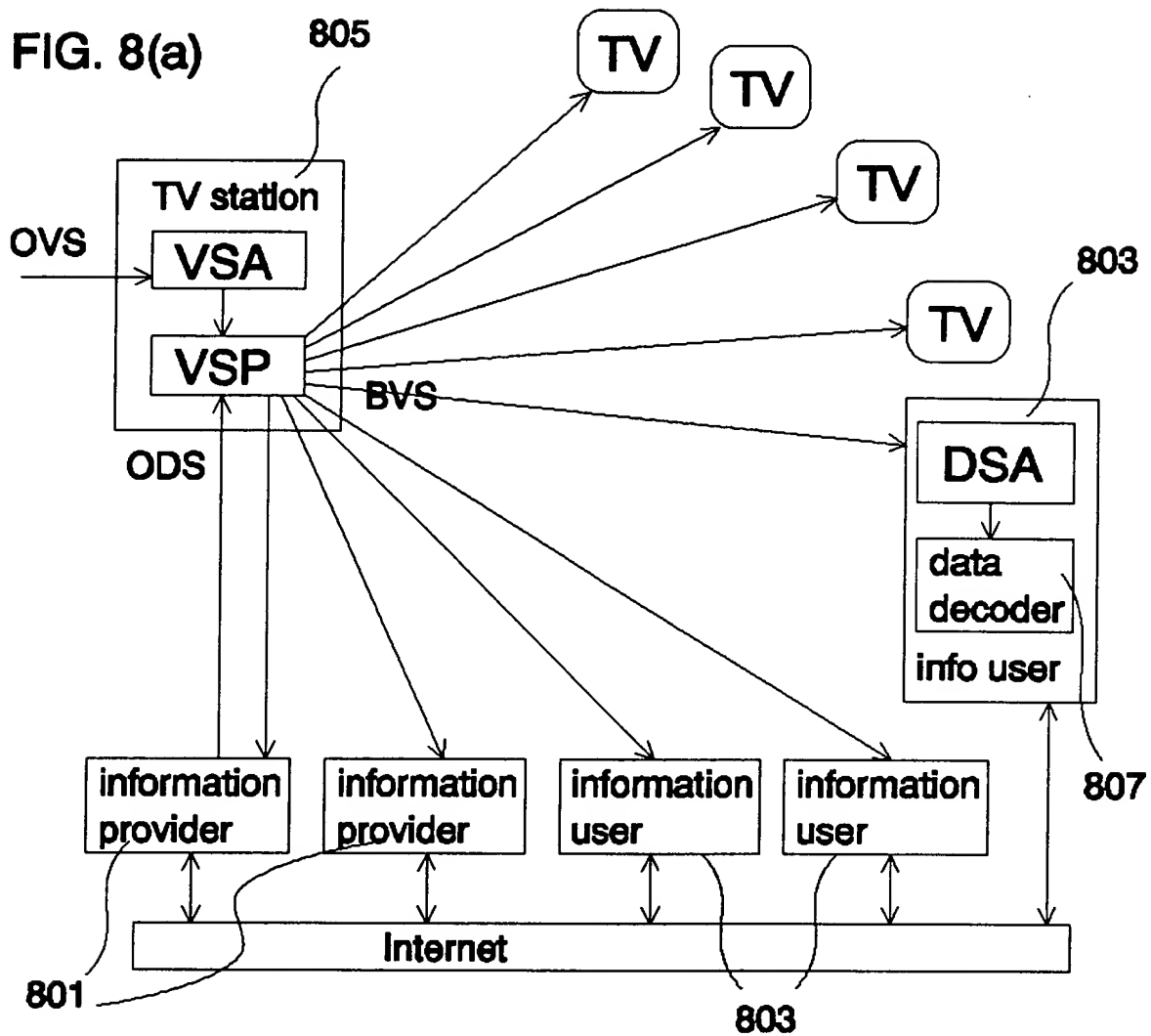
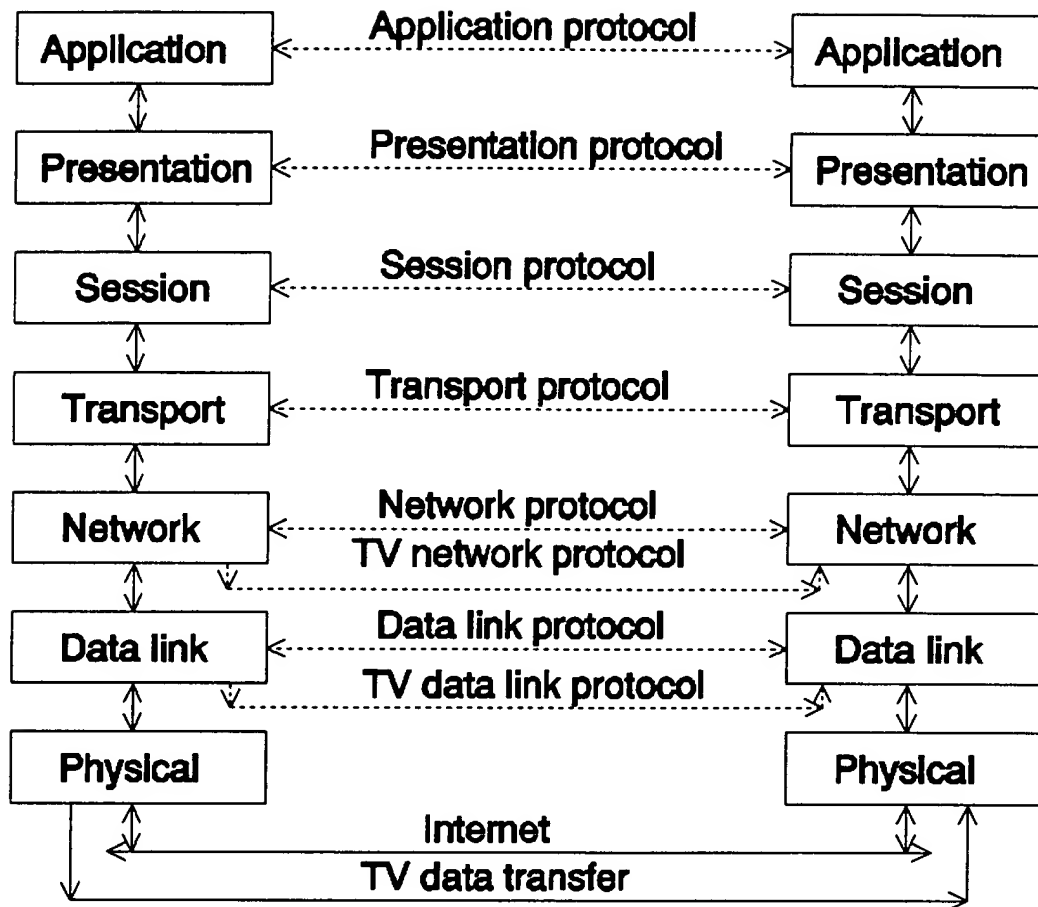


FIG. 8(b)



00000" 60E6E560

FIG. 9(a)

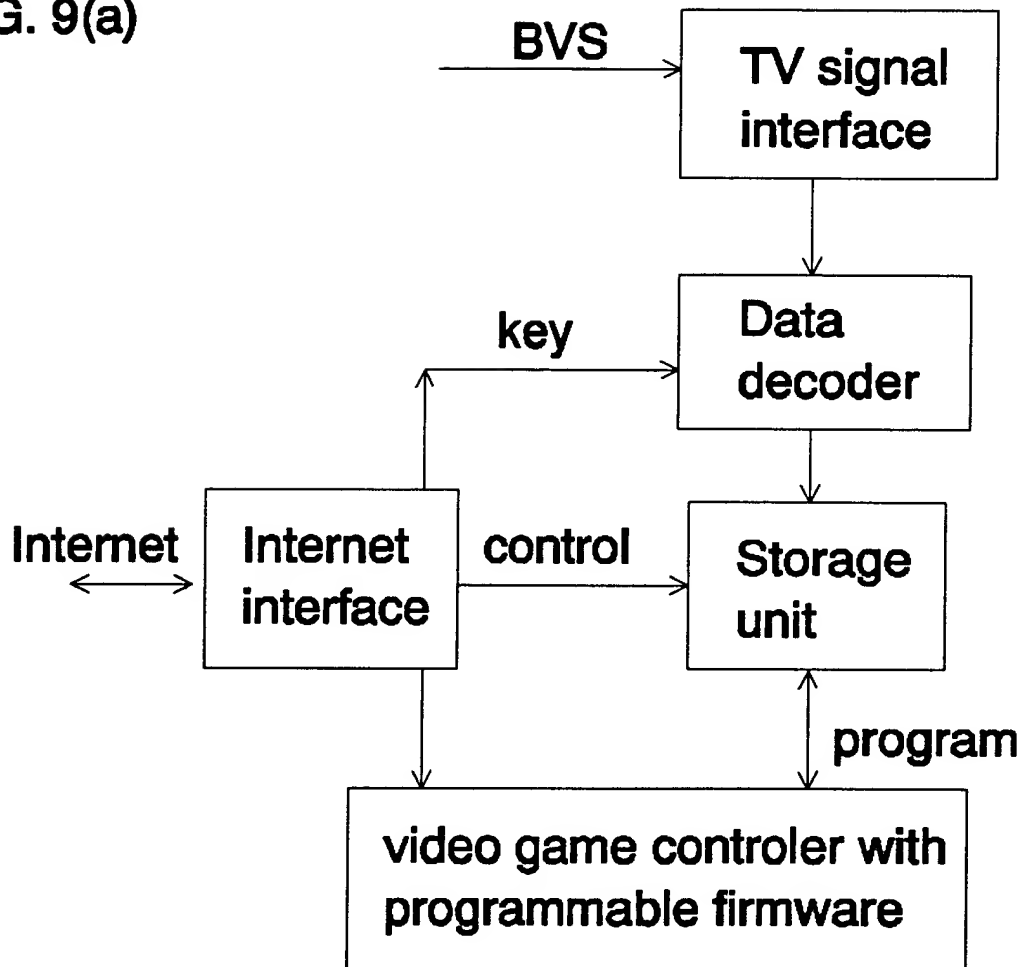
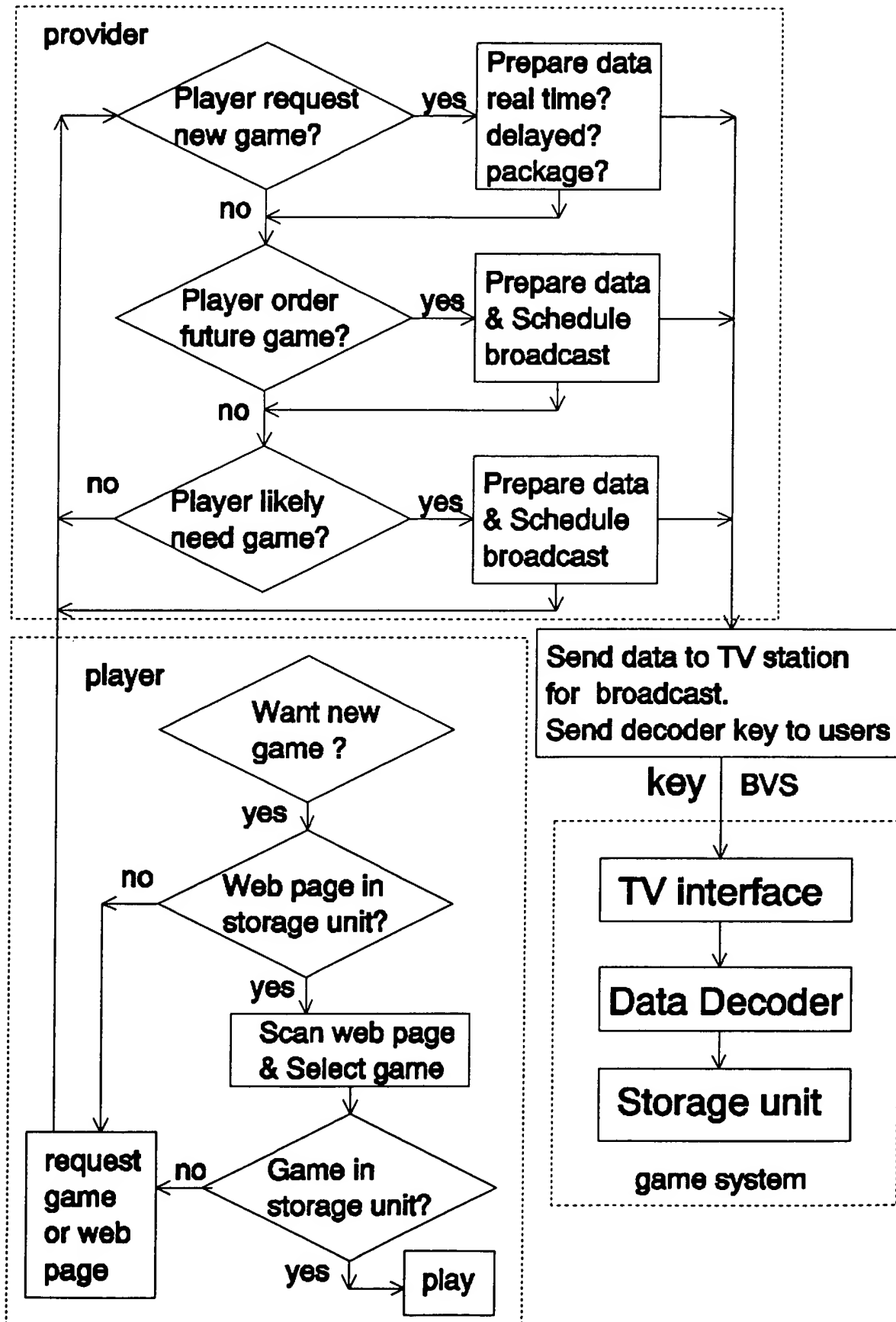


FIG. 9(b)



00000" 00000000

FIG. 10

